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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,149	02/14/2002	Milivoje Aleksic	00100.02:0060(990060D-1)	7928
29153	7590	01/22/2007	EXAMINER	
ADVANCED MICRO DEVICES, INC. C/O VEDDER PRICE KAUFMAN & KAMMHOLZ, P.C. 222 N.LASALLE STREET CHICAGO, IL 60601			DANG, KHANH	
			ART UNIT	PAPER NUMBER
			2111	
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		01/22/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)
	10/075,149	ALEKSIC ET AL.
	Examiner	Art Unit
	Khanh Dang	2111

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 30 November 2006.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 18-20,24 and 25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 18-20, 24, and 25 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO/SB/08)
 Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____

5) Notice of Informal Patent Application

6) Other: _____

DETAILED ACTION

Notice to Applicants

This application, previously been assigned to and examined by Ex. Justin King, is now assigned to Ex. Dang. Any future contact should be directed to Ex. Khanh Dang whose contact information is provided at the end of this Office Action.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the so-called “high speed bus arbiter” and “low speed bus arbiter” (claims 18 and 24) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled “Replacement

Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

Claims 18-20 and 24-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 18, the language "the low speed arbiter supports a lower bus rate than the high-speed bus arbiter" is unclear. As disclosed at least in page 6 of the originally specification, it is the high speed bus that supports the low bus rate and it is the high speed bus that supports the high bus rate. As disclosed and is also well-known, the arbiter simply provides arbitrations, whether between the high speed devices or low speed devices connected to the low speed bus or high speed bus, respectively.

In claim 24, the language "the low speed arbiter supports a lower bus rate than the high-speed bus arbiter" is unclear. As disclosed at least in page 6 of the originally specification, it is the high speed bus that supports the low bus rate and it is the high speed bus that supports the high bus rate. As disclosed and is also well-known, the arbiter simply provides arbitrations, whether between the high speed devices or low speed devices connected to the low speed bus or high speed bus, respectively.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

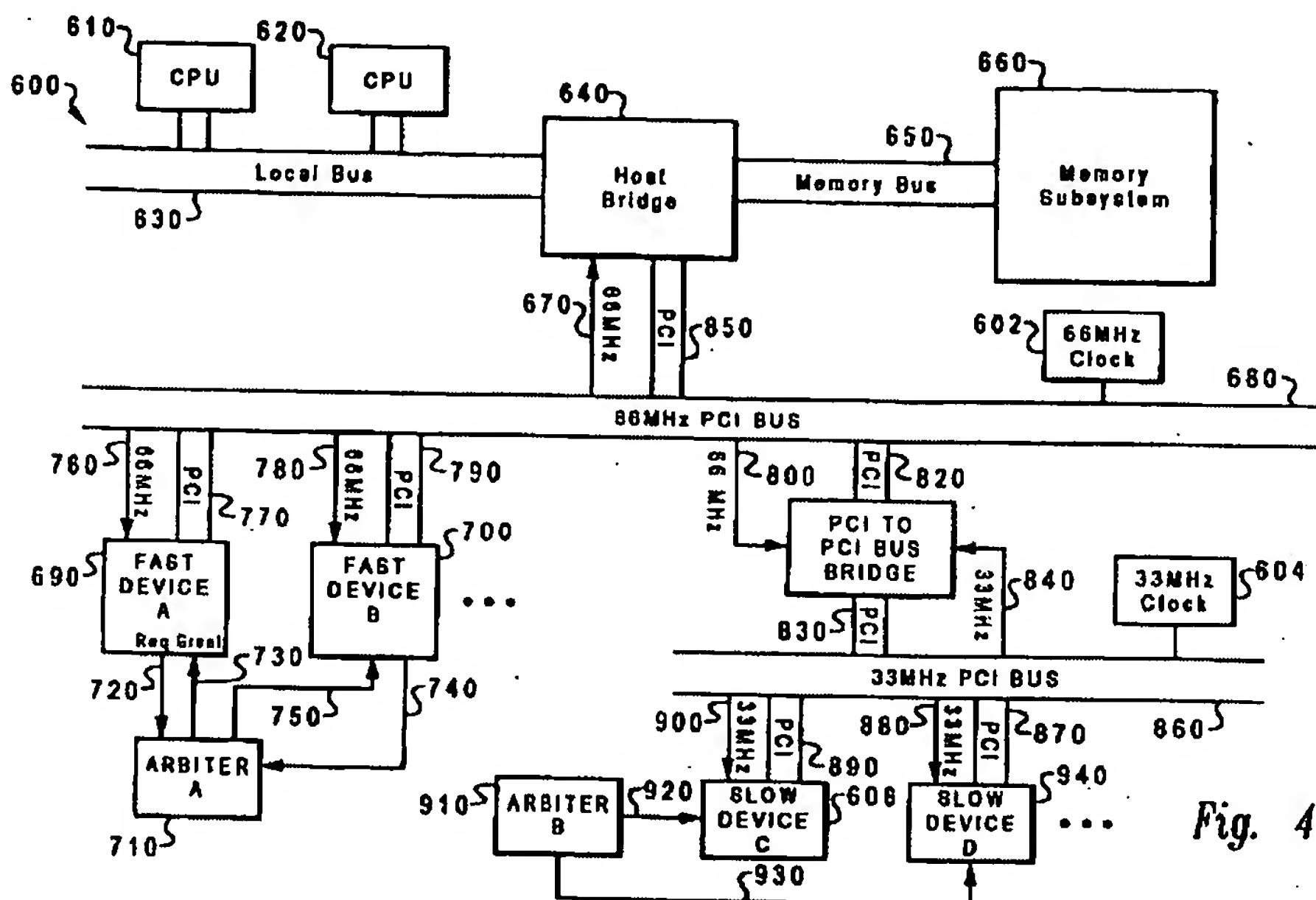
(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 18-20, 24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iachetta Jr. (Iachetta, 5,727,171) in view of Porterfield and Ajanovic et al. (Ajanovic), and Heil et al. (Heil).

Iachetta discloses a data processing system as shown below in Fig. 4:

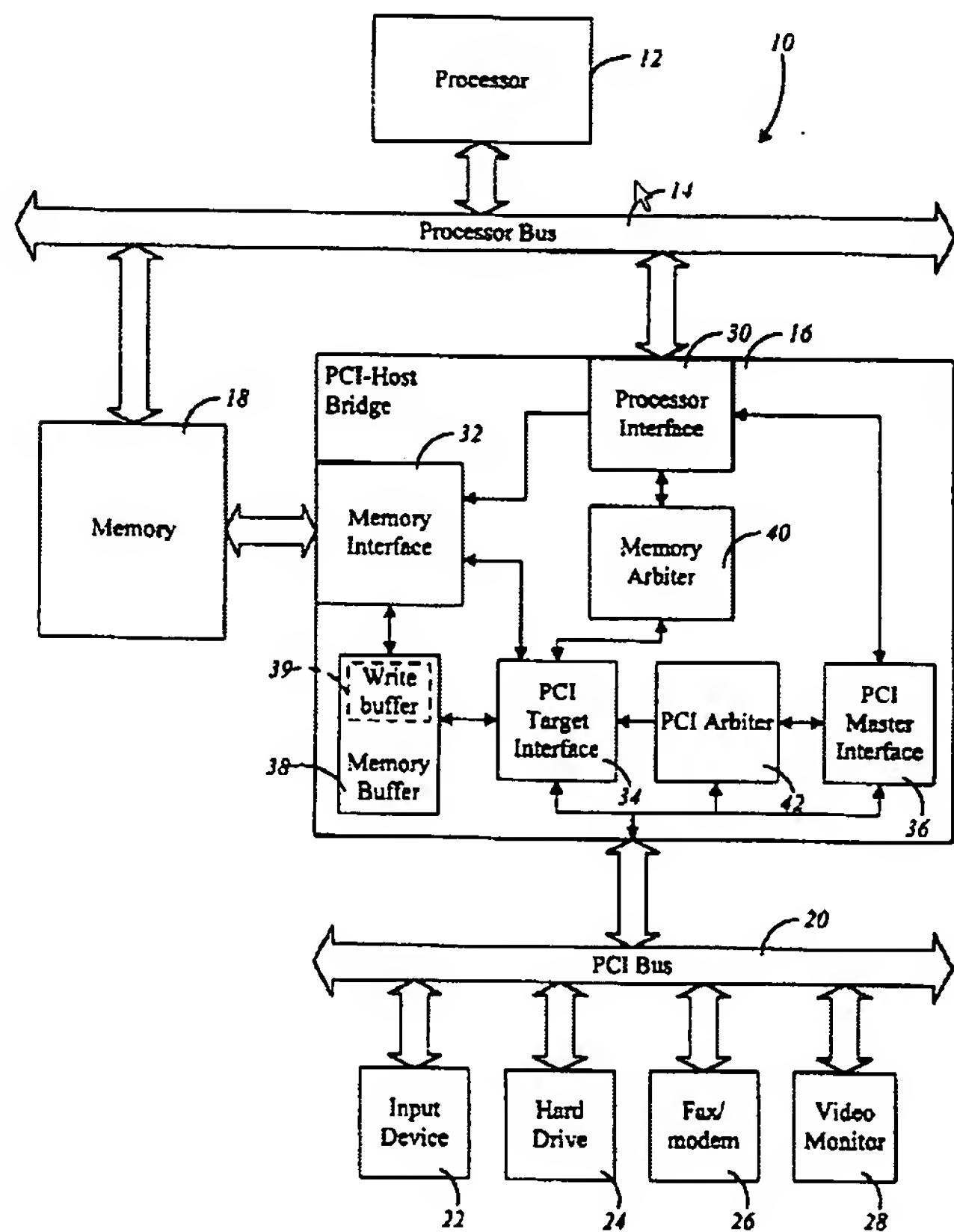


comprising:

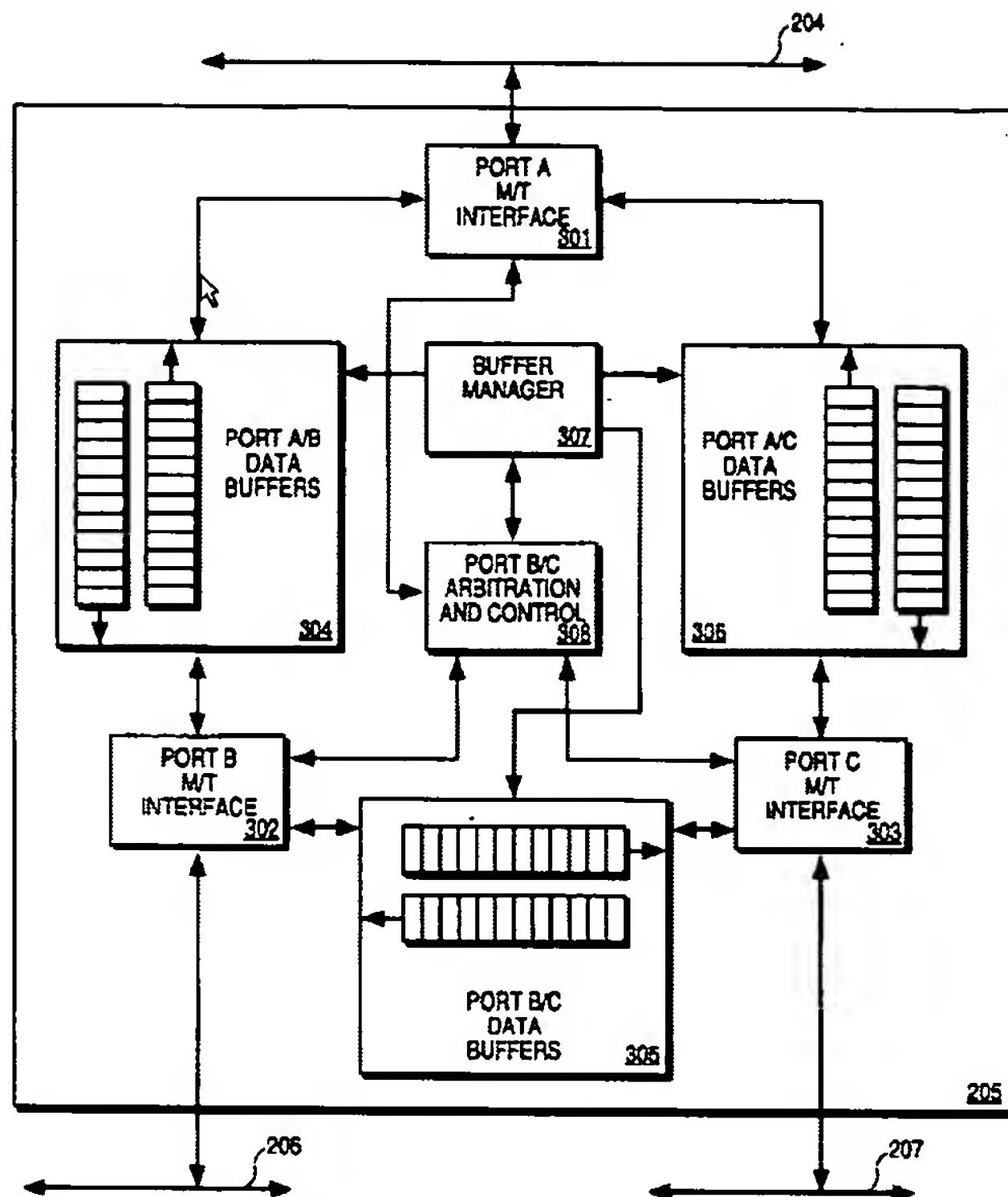
a system controller or host bridge 640 connected to memory 660 via a memory bus 650, a high speed arbiter 710 for providing arbitration to high speed devices A and B, an I/O controller or PCI/PCI bus bridge 810 coupled to a high speed bus 680, a low speed arbiter 910 for providing arbitration to low speed devices C and D; the PCI/PCI bridge 810, the fast devices A and B are all connected to high speed bus 680.

Izchetta does not disclose that the high speed arbiter may be included in the system controller or host bridge 640; and the low speed arbiter may be included in the I/O controller or PCI/PCI bridge 810.

However, the inclusion of an arbiter into the host bridge is old and well-known as evidenced by at least Porterfield. Porterfield disclose the use of an integrated arbiter 42 in a host bridge 16 as shown below:



Further, the inclusion of an arbiter into a PCI bridge 205 is also well-known as evidenced from Ajanovic. Ajanovic discloses an arbiter included in a PCI bridge 203:

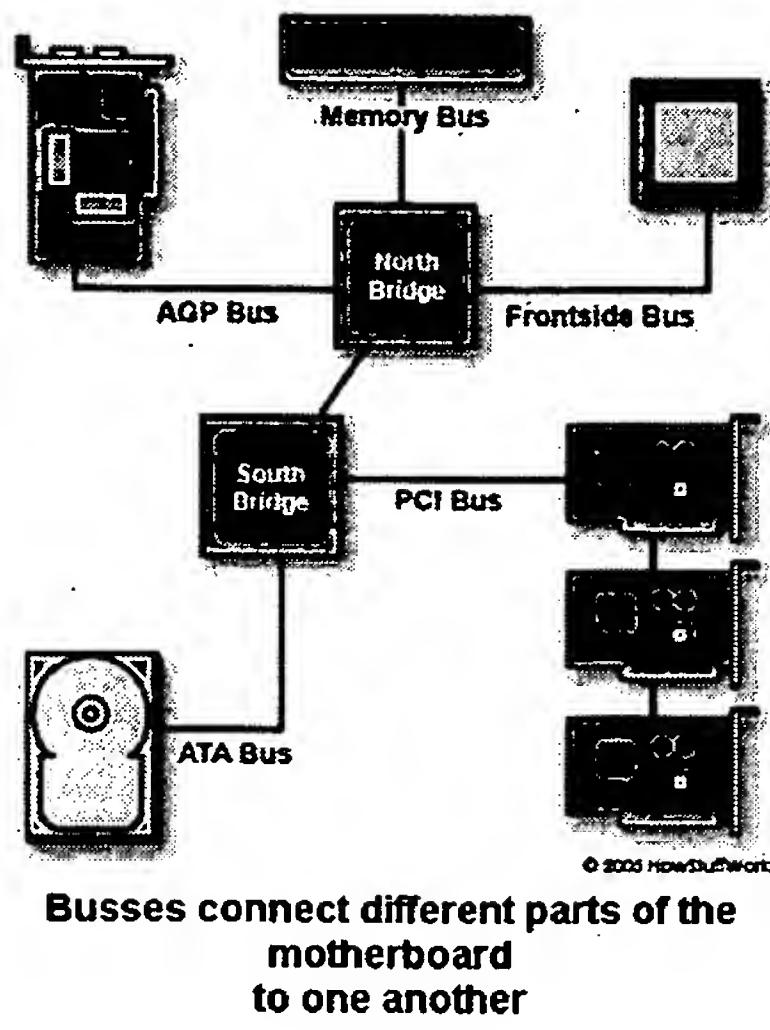


Since all references are both from the same field of endeavor, the purpose disclosed by Porterfield and Ajanovic would have been recognized in the pertinent art of Iachetta.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the high speed arbiter and low speed arbiter into the I/O controller or PCI bridge and system controller or host bridge, respectively, as taught by Porterfield and Ajanovic, for the purpose of reducing the number of discrete components, and thus, reducing cost; and also facilitating system integration. It is important to note that since the PCI bridge, the high speed devices A and B are all connected to the 66 Mhz high speed bus, it is clear only one device can access to the 66 Mhz bus at a time, and the high speed arbiter will provide arbitration to the PCI

bridge, the high speed device A nad the high speed device B for accessing bthe 66 Mhz high speed bus.

The further difference between the claim subject matter and lachetta is the use of dual channel memory controller. However, the use of dual channel memory controller, first developed by Intel, is old and well-known, as evidenced by at least Heil. Heil discloses a multiple-port structure. Heil discloses two separate memory channel controllers (figure 8, structures 134, 136, 142, and 144). Heil teaches that the general access latency caused by the severe bandwidth constraint can be improved with the dual memory channels (column 1, lines 52-56). Thus, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Heil's teachings into lachetta for the purpose of improving the general access latency by the dual memory channels. Note also that it is inherent that a computer system, such as the system disclosed by lachetta must include a hard drive, and the hard drive is connected to the PCI bridge or PCI south bridge. See diagram below from How Motherboards Work, cited below. Note also that ATA Bus is operated as a higher speed than the low PCI Bus (33 Mhz).



With regard to claim 24, see discussion above.

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over lachetta Jr. (lachetta, 5,727,171) in view of Porterfield and Ajanovic et al. (Ajanovic), and Heil et al. (Heil) as applied to claims 18-20 above, and further in view of the following.

The further diffence between the claim subject matter and that of lachetta is the use of the integrated graphics engine into the host bridge or north bridge. However, the use of integrated graphics in the norther bridge is old and well-known as evidence by the definition of north bridge by Wikipedia cited below.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the graphics engine into the north or host bridge of lachetta, since the use of integrated graphics in the norther bridge is old and well-known as evidence by the definition of north bridge by Wikipedia cited below, for the purpose of

reducing the number of discrete components, and thus, reducing cost; and also facilitating system integration.

Response to Arguments

Applicants' arguments filed 11/30/2006 have been fully considered but they are moot in view of the new ground of rejections.

Note that the rejection under 35 USC 112, 1ST paragraph has been withdrawn in view of Applicants' amendment.

Relevant Art

US Patent Nos. 6,175,888 to Guthrie et al., 6,480,917 to Moertl et al., and 6,175,889 to Olarig are cited as relevant art.

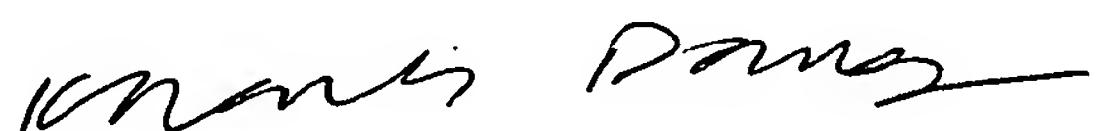
Non Patent Literature/Printed documents: Definitions of North Bridge, South Bridge, RDRAM , Intel 810 Chipset Review, and How Motherboards Work are also cited as relevant art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Dang whose telephone number is 571-272-3626. The examiner can normally be reached on Monday-Friday from 9:AM to 5:PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart, can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Khanh Dang
Primary Examiner